AXI Interface Description

The AXI interface contains a read and write address, data, and write response channels which access the control, status, interrupt, and data register banks in order to interface with the SPI module. Three instance generics determine address bus, data bus, and slave select bus widths. The ACLK clock input and ARESETN active low reset input control global system operation.

Read Operations

*Address Channel*

The ARADDR signal controls which register is being read from. The corresponding chip select signal is set when the ARVALID signal is set, indicating that read address and control information is valid. The ARVALID signal remains high until the address acknowledgement signal ARREADY is set high. The ARREADY signal indicates the slave is ready to accept the signals, launching the broadcasting process.

*Data Channel*

RDATA vector is the read data output. The RVALID signal indicates that the read data is available for the transfer. The RREADY signal indicates that the master can accept the data and response information. The RRESP vector indicates the status of the transfer.

Write Operations

*Address Channel*

The AWADDR signal controls which register is being written to. The corresponding chip select signal is set when the AWVALID signal is set, indicating that write address and control information is valid. The AWREADY signal indicates the slave is ready to accept the address and control signals, launching the transfer process.

*Data Channel*

WDATA signal is the write data input. WSTB signal vector input is the write strobes, determining which byte lanes are being updated. WVALID indicates the data and strobes are available for the transaction. WREADY indicates the slave can accept the write data.

*Response Channel*

The BRESP signal indicates the status of the write transaction.

FSM

The AXI interface will have a 3 state FSM including wait, broadcast, and writing.

The address valid signals determine if a read or write is to be made, at which point the corresponding data valid signal is set. The slave ready signal then controls the latching of read or write data from/to the addressed register. After the transaction is complete, the response signal is output, and the acknowledgement signal is reset.